



- 1 -

Docket: 0756-1173

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT application of )  
Masaaki HIROKI et al. )  
Serial No. 08/372,899 ) Art Unit: 2609  
Filed: January 17, 1995 ) Examiner: L. Lao  
For: Electro-Optical Device )

RECEIVED  
AUG 26 97  
GROUP 2600

APPEAL BRIEF

Honorable Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

In accordance with the provisions of 35 U.S.C. § 134 and 37 C.F.R. § 1.192(a), Appellants submit this Appeal Brief in triplicate to appeal the examiner's final rejection of claims 21-31 and 34-35 in the Official Action mailed October 28, 1997.

CERTIFICATE OF MAILING

I hereby certify that the correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 7-28-97.  
*Close n. J. o'Neil*

**TABLE OF CONTENTS**

I.	REAL PARTY IN INTEREST .....	3
II.	RELATED APPEALS AND INTERFERENCES .....	3
III.	STATUS OF CLAIMS .....	3
IV.	STATUS OF AMENDMENTS .....	4
V.	SUMMARY OF INVENTION .....	4
VI.	STATEMENT OF ISSUES .....	5
VII.	GROUPING OF CLAIMS .....	5
VIII.	ARGUMENTS .....	5
IX.	APPENDICES .....	13

**I. REAL PARTY IN INTEREST**

The named inventors have assigned all ownership rights in the pending application to Semiconductor Energy Laboratory Co., Ltd., 398, Hase, Atsugi-shi, Kanagawa-ken, 243 Japan, which is the real party in interest.

**II. RELATED APPEALS AND INTERFERENCES**

The appellants, their legal representatives, and the assignee are not aware of any other pending appeals or interferences which will directly affect or be directly affected by, or have a bearing on the Board's decision in this appeal. Applicants are aware of an appeal in which a decision was rendered in Application Serial Number 07/885,637 (Appeal No. 95-1672), a copy of which is attached hereto. As discussed in detail below, it is believed that the issues found dispositive in this related appeal are dispositive here as well.

**III. STATUS OF THE CLAIMS**

Claims 21-31 and 34-35 are pending in the present application and claims 21, 26, and 31 are independent. No claims have been deemed allowable by the examiner. Claims 21-31 are rejected as obvious based on the combination of U.S. Patent 5,408,246 to Inaba et al., U.S. Patent 5,414,443 to Kanatani et al. and either applicant's prior art or U.S. Patent 4,873,516 to Castleberry. Claim 34 is rejected as obvious based on Inaba et al., Kanatani et al. and either applicant's prior art or Castleberry as applied to claims 21-31 and U.S. Patent 5,142,272 to Kondo. Claim 35 is rejected as obvious based on the combination of Inaba et al., Kanatani et al., Kondo and either applicant's prior art or Castleberry as applied to claim 34 and Danayama et al. (apparently U.S. Patent 4,897,639 to Kanayama et al.) and Kondo (apparently a second citation to U.S. Patent 5,142,272).

**IV. STATUS OF AMENDMENTS**

No claim amendments were filed in response to the Final Official Action mailed October 28, 1996 and all amendments are believed to have been entered in the present application. Thus, the status of the claims in this application is as set forth above and in Appendix A.

**V. SUMMARY OF THE INVENTION**

The present invention is directed to a method of driving an active matrix device. More specifically, the present invention is directed to a method of driving an active matrix device wherein a scan signal is used to address a thin film transistor for a predetermined period that is time divided into a predetermined number of divisions and a data signal having a plurality of constant width pulses indicative of a gradation to be displayed at a pixel electrode of the device are applied to a pixel electrode during the predetermined scan period such that an average voltage of the pulses that have been applied to each of the pixel electrodes during the predetermined period is applied to a corresponding one of the pixel electrodes after the predetermined period (Page 5, lines 9-18 and Figure 1).

As shown in Figure 1, during a period "t", i.e. while scanning a gate line  $X_1$ , a predetermined number of pulses having a constant pulse width are applied to a data line  $Y_1$  so that pulses are applied to a pixel A during the period "t". Depending upon the number of pulses 227, the voltage 228 applied to the pixel A during a non-selected period is determined. Accordingly, a gradation in pixel A can be achieved by changing the number of pulses to be applied to a data line during the scanning period "t."

As seen in independent claims 21, 26 and 31, the present invention is further distinguished over the cited references in that an average voltage of the pulses that have been applied to each of the pixel electrodes during a predetermined period is applied to a corresponding one of the pixel electrodes after the predetermined period to display a tone of an image (Page 5, lines 14-18 and Figure 1). This feature results in a system and

method that does not decrease display frequency and thus enables a display of high quality (See page 3, last line through page 4, line 6 and page 4, lines 12-17).

Thus, the present invention provides a method of driving an active matrix device wherein a data signal having (1) a plurality of constant width pulses indicative of a gradation to be displayed at a pixel electrode of the device are applied to a pixel electrode during (2) a predetermined scan period such that (3) an average voltage of the pulses that have been applied to each of the pixel electrodes is applied to a corresponding one of the pixel electrodes after the predetermined period.

## **VI. STATEMENT OF ISSUES**

- A. Whether claims 21-31 are unobvious in view of the combination of U.S. Patent 5,408,246 to Inaba et al., U.S. Patent 5,414,443 to Kanatani et al. and either applicant's prior art or U.S. Patent 4,873,516 to Castleberry.
- B. Whether claim 34 is unobvious in view of the combination of Inaba et al., Kanatani et al. and either applicant's prior art or Castleberry as applied to claims 21-31 and U.S. Patent 5,142,272 to Kondo, and whether claim 35 is unobvious in view of the combination of Inaba et al., Kanatani et al., Kondo and either applicant's prior art or Castleberry as applied to claim 34 and U.S. Patent 4,897,639 to Kanayama et al.

## **VII. GROUPING OF CLAIMS**

The rejected claims shall stand or fall together.

### **VIII. ARGUMENTS**

- A. Whether claims 21-31 are unobvious in view of the combination of U.S. Patent 5,408,246 to Inaba et al., U.S. Patent 5,414,443 to Kanatani et al., and either applicant's prior art or U.S. Patent 4,873,516 to Castleberry.

The Official Action rejects claims 21-31 as obvious based on the combination of U.S. patent 5,408,246 to Inaba et al., U.S. Patent 5,414,443 to Kanatani et al. and either applicant's prior art or U.S. Patent 4,873,516 to Castleberry. The Official Action appears to rely primarily on Inaba et al. for teaching the application of a plurality of pulses during a scan period as recited in the currently pending claims, and cites column 8, lines 4-9 in support of this rejection. This portion of Inaba et al. reads:

In the above example, a driving mode for gradational display through pulse amplitude modulation was adopted, but the present invention is also applicable to other known driving modes wherein the pulse duration or pulse number is varied depending on given gradation data.

In an Advisory Action mailed in response to an After Final Response filed April 14, 1997, the Examiner clarified that "Inaba et al. teach a plurality of pulses are applied during the scanning period of a gate line (S1, S2) (see figure 9)."

The Official Action admits that Inaba fails to disclose a thin film transistor as claimed, and relies on the teachings of Kanatani for disclosing this feature of the present invention. As motivation for combining the teachings of Inaba and Kanatani, the Official Action states "it would have been obvious to have modified Inaba et al. with the teachings of Kanatani et al, so to have a switch element to turn the pixel ON or OFF in a liquid crystal display."

The Official Action further admits that this combination of Inaba and Kanatani fails to teach the application of an average data signal to a data electrode as recited in the claims of the present application. The Official Action relies on the admitted prior art (figure 11 and page 5, lines 21-27) or Castleberry for teaching these features and asserts it would be obvious to combine them with the combination of Inaba and Kanatani "so as to eliminate cross-talk in a thin film transistor matrix addressed liquid crystal display."

To establish a *prima facie* case of obviousness, (1) there must be some suggestion or motivation (either in the references themselves or in the knowledge generally available to one of ordinary skill in the art) to combine the reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art references when combined must teach or suggest all the claim limitations. See *MPEP* § 2142-43. Once a *prima facie* case of obviousness has been made by the Patent Office, the burden then shifts to Applicant to rebut that *prima facie* case. This rebuttal can include any arguments or presentation of evidence that is pertinent to the issue of unobviousness including, for example, comparison of test data showing unexpected properties not present in the prior art or that the prior art is so deficient that there is no motivation to make what might appear to be obvious changes. See *In re Dillon*, 16 U.S.P.Q.2d 1897, 1901 (Fed. Cir. 1990); *MPEP* § 2142.

As noted above, *MPEP* § 2143 makes clear that in order for a *prima facie* case of obviousness to be established, the combination of references must "teach or suggest all of the claim limitations." "The references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious." *Ex parte Clapp*, 227 USPQ 972,973 (Bd. Pat. App. & Inter. 1985). When the motivation to combine the teachings of the prior art references is not immediately apparent, the examiner has the duty of explaining why the combination of the references is proper. *MPEP* § 2142.

This burden of establishing a *prima facie* case of obviousness clearly has not been met in this case. First, the combination of Inaba, Kanatani and either the admitted prior art or Castleberry clearly does not "teach or suggest" all of the claim limitations when considering the teachings of these references as a whole. The prior art of record, and more specifically Inaba, fails to disclose application of a plurality of pulses during the scanning period of a gate line. That is, claim 21 for example, recites addressing a TFT with a scan signal for a predetermined period, supplying a data signal through the TFT during addressing with the scan signal, wherein the data signal contains a plurality of

pulses having a constant pulse width and wherein an average voltage of the pulses is applied to the pixel electrode after the predetermined period. Thus, claim 21 makes clear that the plurality of pulses are applied during a single, predetermined scan period.

Inaba et al., to the contrary, does not disclose that a plurality of pulses are applied during a scan period, and clearly does not disclose that an average voltage of these pulses is applied after the predetermined scanning period as further recited in claim 21. Figure 9 of Inaba relied on in the Advisory Action clearly demonstrates that a single pulse is applied during each scan period. This can be seen by comparing the timing diagrams for the three scanning lines S1-S3 with the timing diagram for the data line I. As can be seen, scanning lines S1-S3 are sequentially addressed by the application of a 16 volt pulse. During each of these addressing periods, data line I is supplied with a single pulse. The "reset pulses" shown applied to scan lines S1-S3 are relevant to the specific driving method disclosed in Inaba et al., but do not appear to have any relevance to the presently claimed invention. Thus, Figure 9 and the accompanying description do not appear to even remotely disclose or suggest the claimed application of a number of pulses during the scanning period of a gate line.

Admittedly, column 8, lines 4-9 summarily states that the invention of Inaba is also applicable to other known driving modes wherein the pulse duration or pulse number is varied depending on given gradation data. Beyond this, however, Inaba does not provide any details whatsoever as to what these "other known driving modes" involve. Thus, it is not at all clear from Inaba if these "other known modes" include a plurality of pulses applied during a scan period as claimed. Importantly, Inaba does not disclose or suggest that the single pulses applied during the scan period shown in Figure 9 thereof should merely be replaced with a number of pulses. Instead, Inaba discloses that "known driving modes" where the pulse number is varied could be employed. No reference disclosing any such "known driving mode," however, appears to have been located during the search of the Patent Office's records. Thus, it is clear that the invention of Inaba et al. is not concerned with any specific driving method and therefore Inaba fails to disclose the details of any particular driving method, referring only generally to "other known driving

modes." Thus, for this first reason, it is respectfully submitted that without more, one of skill in the art, taking the teachings of Inaba as a whole, would clearly not be taught to employ a plurality of pulses during a scan period and that a *prima facie* case of obviousness cannot be maintained.

Furthermore, the present claims recite that the predetermined scan period is time-divided into a predetermined number of divisions and the data signal contains a plurality of pulses having a constant pulse width. Not only is the prior art of record devoid of any disclosure or suggestion that a plurality of pulses having a constant pulse width should be used, but this feature of the present invention is not squarely addressed in the Official Action. While the Official Action notes that the data signal of Inaba has a plurality of pulses with a constant pulse width, it is clear from even a cursory review of Figure 9 that these pulses are applied during different scan periods S1, S2 and S3. Even if column 8, lines 4-9 could be said to suggest that a plurality of pulses should be applied during a single scan period, it clearly does not suggest that these pulses should have a constant pulse width. Therefore, for this second reason, it is respectfully submitted that a *prima facie* case of obviousness cannot be maintained.

Also, the first prong noted above -- that there must be some suggestion or motivation (either in the references themselves or in the knowledge generally available to one of ordinary skill in the art) to combine the reference teachings -- has clearly not been met in this case. When the motivation to combine the teachings of the prior art references is not immediately apparent, the examiner has the duty of explaining why the combination of the references is proper. MPEP § 2142.

With respect to the first combination, the Official Action asserts that one of skill in the art would be motivated to combine the teachings of Inaba and Kanatani so to have a switch element to turn the pixel ON or OFF in a liquid crystal display. This alleged "motivation" is respectfully traversed in that one of skill in the art need look no farther than Inaba itself to accomplish this objective. That is, Inaba discloses a driving method for an electro-optical modulating apparatus that includes a "voltage application circuit" for applying a voltage to a pixel so as to display a halftone (Abstract and column 2, line

55 - column 3, line 3). It is not clear why one of skill in the art would look to Kanatani to have a switch element to turn the pixel ON or OFF in a liquid crystal display when that functionality is apparently already taught by Inaba. The Official Action has not provided any convincing line of reasoning as to why one of skill in the art would be motivated to look to Kanatani. Importantly, just because the references could be combined does not mean that they should be. Therefore, absent some further suggestion or motivation to one of skill in the art to combine the teachings of Inaba and Kanatani, it is believed that a *prima facie* case of obviousness has not been made.

As noted above, Applicant is also aware of a Decision of the Board of Appeals in Application Serial Number 07/885,637 (Appeal No. 95-1672), a copy of which is attached hereto. In this decision, an issue similar to that relevant here was decided and the Board found the specific relationship between the application of signals to the scan and data lines to be dispositive. In that case, the claims recited that a specific signal was applied between the application of a reference signal to one address line and the application of the reference signal to the next address line. The reference relied on by the Examiner, however, disclosed the application of specific signals during a period after all the reference signals had been applied to the address lines, rather than during a period between application of the reference signals to the address lines. Thus, the board found the specific relationship between the application of signals to the scan and data lines to be dispositive and reversed the rejection of the claims in that matter.

It is believed that a similar line of reasoning can be applied to the present application. That is, the present invention clearly recites a specific relationship between the application of signals to the scan and data lines. The prior art of record relied on to reject these claims, however, fails to disclose or suggest this specific claimed relationship of these signals. Thus, for all of the above reasons, reversal and allowance of claims 21-31 is respectfully requested.

B. Whether claim 34 is unobvious in view of the combination of Inaba et al., Kanatani et al. and either applicant's prior art or Castleberry as applied to

claims 21-31 and U.S. Patent 5,142,272 to Kondo, and whether claim 35 is unobvious in view of the combination of Inaba et al., Kanatani et al., Kondo and either applicant's prior art or Castleberry as applied to claim 34 and Danayama et al. (apparently U.S. Patent 4,897,639 to Kanayama et al.) and Kondo (apparently a second citation to U.S. Patent 5,142,272).

The outstanding rejections of claims 34 and 35 rely in part on the rejections of claims 21-31 discussed above and are believed to be in error for all of the same reasons as discussed above with respect to those claims. Reversal and allowance of these claims is requested for all of the same reasons previously discussed.

For all of the above reasons, it is respectfully asserted that the pending claims of the present application are unobvious in view of the prior art of record. Reversal of the outstanding rejections of record and allowance of the claims of this application is requested.

Respectfully submitted,



Eric J. Robinson  
Reg. No. 38,285

Sixbey, Friedman, Leedom & Ferguson, P.C.  
2010 Corporate Ridge, Suite 600  
McLean, Virginia 22102  
(703) 790-9110

**IX. APPENDICES**

- A. Claims involved in the appeal.
- B. U.S. Patent 5,408,246 to Inaba et al.
- C. U.S. Patent 5,414,443 to Kanatani et al.
- D. U.S. Patent 4,873,516 to Castleberry.
- E. U.S. Patent 5,142,272 to Kondo
- F. U.S. Patent 4,897,639 to Kanayama et al.
- G. Decision of the Board of Appeals in Application Serial No. 07/885,637  
(Appeal No. 95-1672).

APPENDIX A  
PENDING CLAIMS

21. A driving method for an electro-optical device having a plurality of pixel electrodes, each of which has a light modulating layer and a thin film transistor connected thereto, said method comprising the steps of:

addressing said thin film transistor with a scan signal for a predetermined period, in sequence; and

supplying each of said pixel electrodes with a data signal through the corresponding thin film transistor during said addressing with said scan signal,

wherein said predetermined period is time-divided into a predetermined number of divisions, and said data signal contains a plurality of pulses having a constant pulse width, the number of said pulses being determined depending upon a tone of an image to be displayed, and

wherein an average voltage of said pulses is applied to corresponding one of said pixel electrodes after said predetermined period to display said tone of said image.

22. The method of claim 21 wherein voltage values of said pulses are substantially constant.

23. The method of claim 21 wherein said light modulating layer comprises a liquid crystal.

24. The method of claim 21 wherein said plurality of pixel electrodes are arranged in the form of a matrix.

25. The method of claim 24 wherein the step of addressing said thin film transistor is performed in a line sequence.

26. A driving method for an electro-optical device having a plurality of pixel electrodes, each of which has a light modulating layer and a thin film transistor connected thereto, said method comprising the steps of:

addressing said thin film transistor with a scan signal for a predetermined period in sequence, where said predetermined period is time-divided into a predetermined number of divisions;

preparing an original image data in accordance with an image to be displayed;

converting said original image data into a data signal to be supplied to each of said pixel electrodes where said data signal contains a plurality of pulses having a constant pulse width, the number of said pulses being determined depending upon a tone of the image to be displayed;

supplying each of said pixel electrodes with said data signal through the corresponding thin film transistor during said addressing with said scan signal for said predetermined period,

wherein an average voltage of said pulses is applied to corresponding one of said pixel electrodes after said predetermined period to display said tone of said image.

27. The method of claim 26 wherein voltage levels of said pulses are substantially constant.

28. The method of claim 26 wherein said light modulating layer comprises a liquid crystal.

29. The method of claim 26 wherein said plurality of pixel electrodes are arranged in the form of a matrix.

30. The method of claim 29 wherein the step of addressing said thin film transistor is performed in a line sequence.

31. An electro-optical device comprising:
  - a plurality of pixel electrodes arranged in a matrix form;
  - a thin film transistor connected to corresponding one of said pixel electrodes;
  - addressing means for addressing said thin film transistor with a scan signal for a predetermined period, in sequence;
  - image data production means for producing image data in accordance with an image to be displayed;
  - image data processing means for processing said image data to produce a data signal having a plurality of pulses, the number of said pulses determined depending upon a tone of said image to be displayed; and
  - data signal supply means for supplying said data signal to each of said pixel electrodes during addressing with said scan signal for said predetermined period,
    - wherein said pulses have a constant pulse width, and
    - wherein an average voltage of said pulses is applied to corresponding one of said pixel electrodes after said predetermined period to display said tone of said image.

34. The device of claim 31 wherein said image data processing means includes ROM means for storing gradated display data.

35. The device of claim 34 wherein said data signal supply means includes counter means for forming pulses to drive the electro-optical display and flip-flop means operably connected with said ROM means, said counter means and a clock line for controlling the operation of said counter means.